Abstracts

High-efficiency harmonic loaded oscillator with low bias using a nonlinear design approach

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We present a design method for an optimized high-efficiency harmonic loaded oscillator. The proposed approach predicts the performance of oscillators including output power, dc-RF conversion efficiency, and dc-bias current shift during start-up transition. In this method, the performance of the oscillator can he optimized based on the performance analysis of the active device under the assumed operation conditions. The effects of fundamental and harmonic loading on output power and efficiency are investigated by the proposed approach. Two kinds of stability conditions are addressed for an oscillator initially biased at a low gate voltage. Using the proposed approach, we design an oscillator that has a high efficiency of 61% at 1.86 GHz with a very low bias voltage of 2.0 V.

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